

[0089]

An integrated circuit has a metal layer that includes conductors to provide interconnectivity for components of the integrated circuit chip. The metal layer is divided into at least two sections, such that a first section has a preferred direction and the second section has a preferred wiring direction that is different from the first preferred direction. The first and second preferred directions on a single metal layer may consist of any direction. The metal layer may be divided into more than two sections, wherein each section has a preferred wiring direction. Wiring geometries for multi-level metal layers are also disclosed

## Figures

IC (Top View)

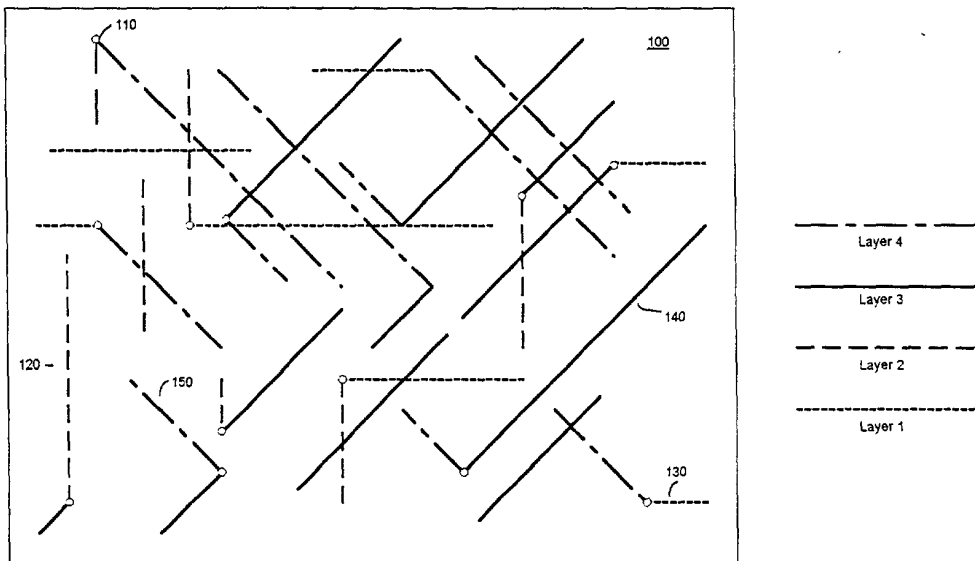


Figure 1a

IC (Top View)

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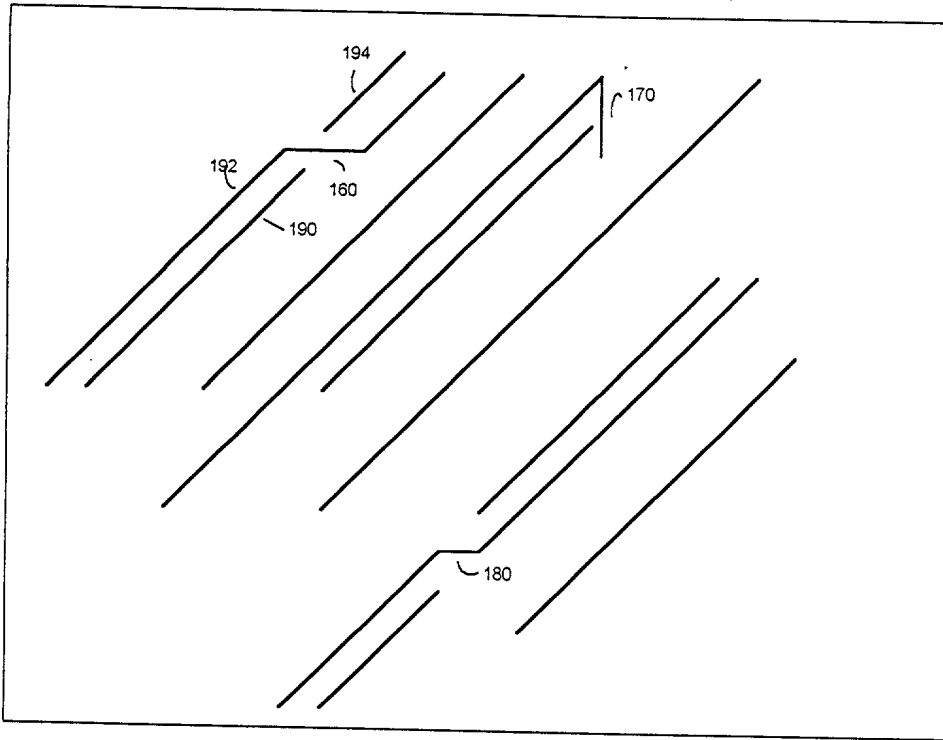
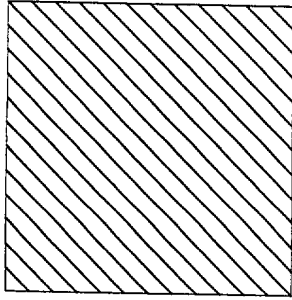
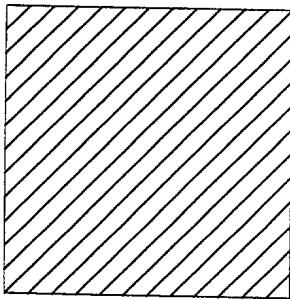


Figure 1b



Layer "n+1"

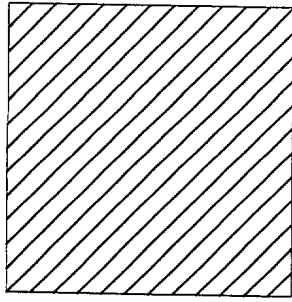
Octalinear (-45 Deg.)



Layer "n"

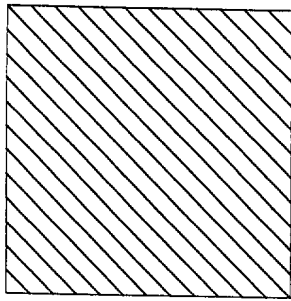
Octalinear (+45 Deg.)

**Figure 2a**



Layer "n+1"

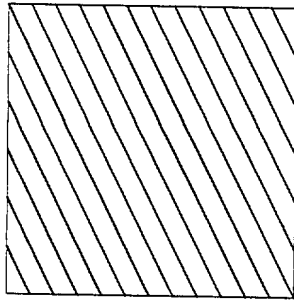
Octalinear (+45 Deg.)



Layer n

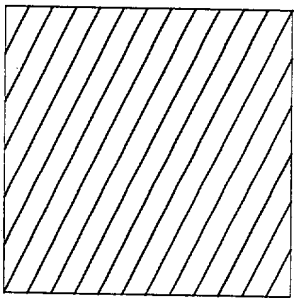
Octalinear (-45 Deg.)

**Figure 2b**



Layer "n+1"

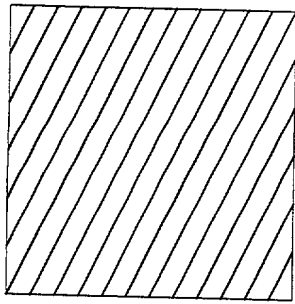
(-60 Degrees)



Layer "n"

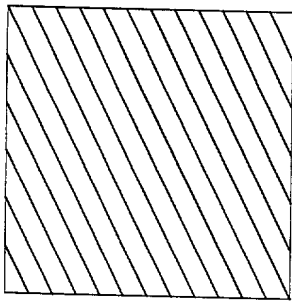
(+60 Degrees)

**Figure 3a**



Layer "n+1"

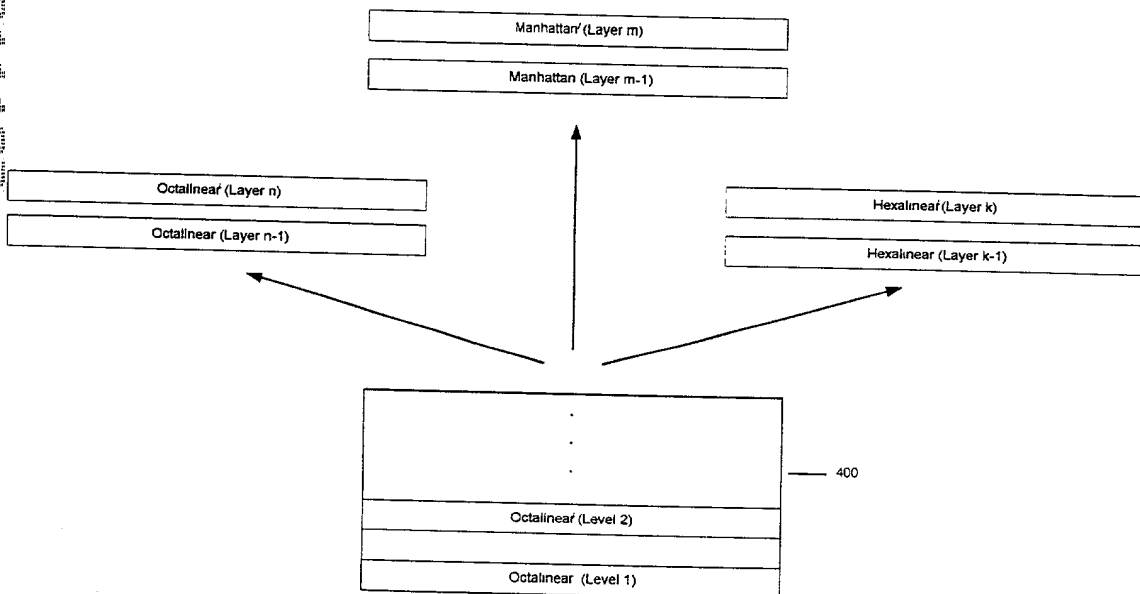
(+60 Degrees)



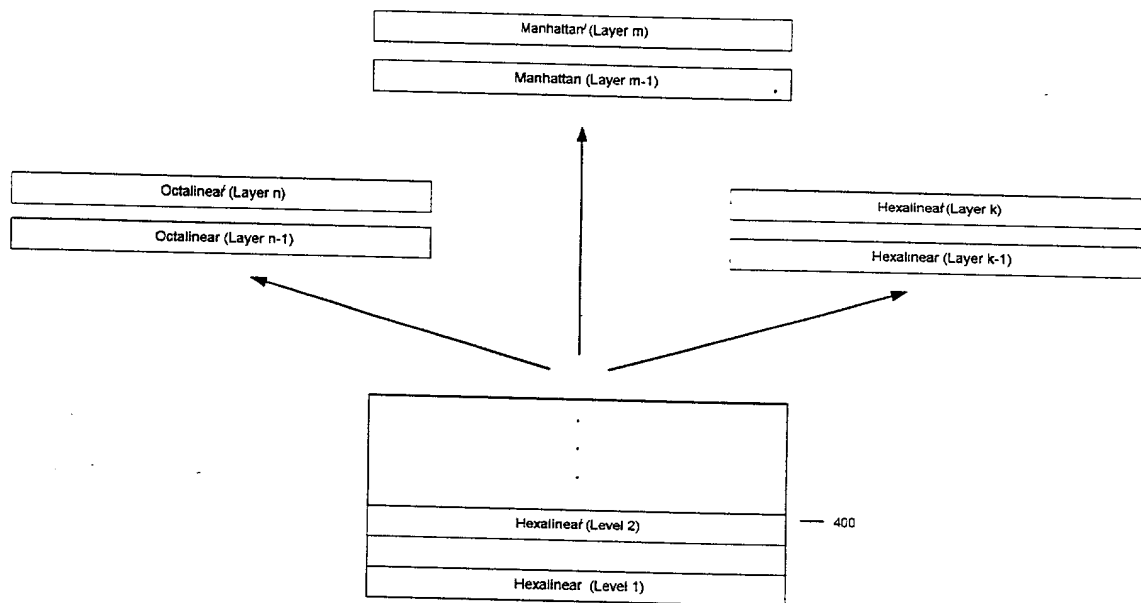
Layer "n"

(-60 Degrees)

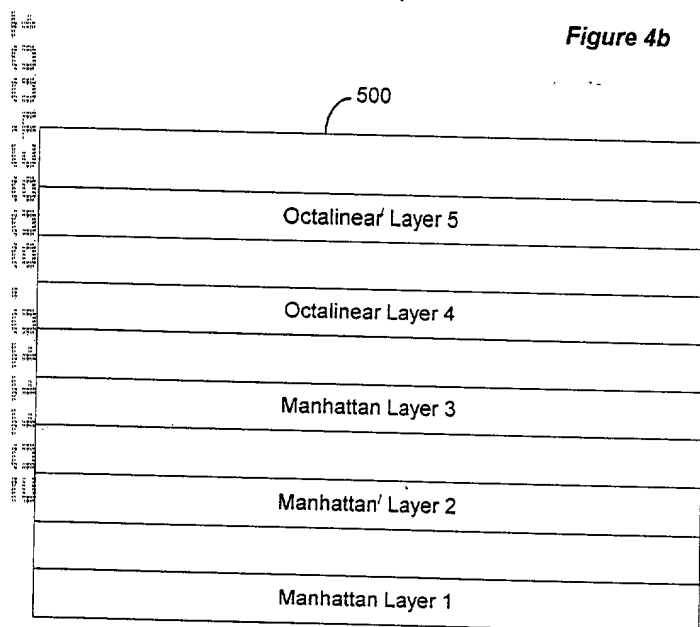
**Figure 3b**



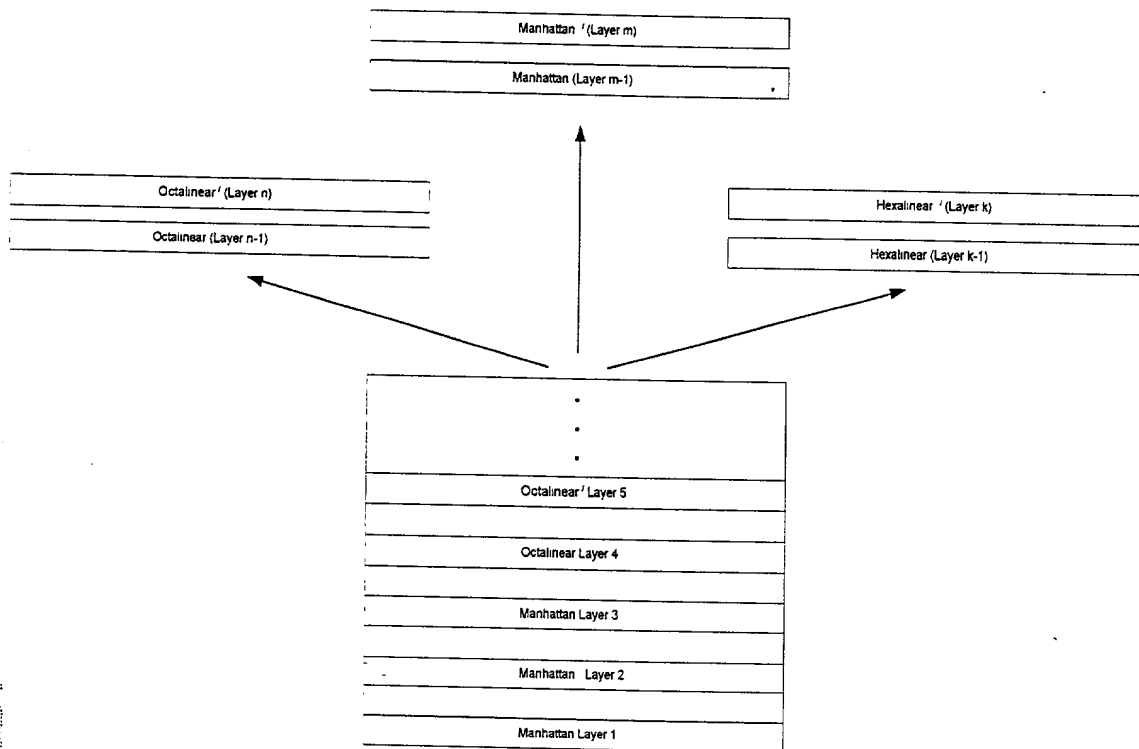
**Figure 4a**



**Figure 4b**

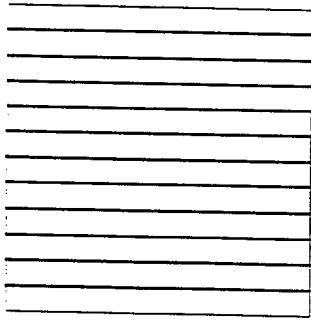


**Figure 5a**



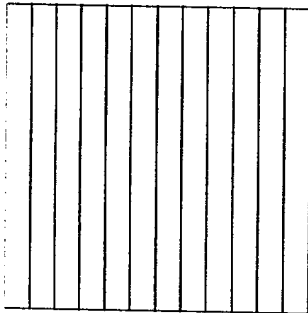
**Figure 5b**





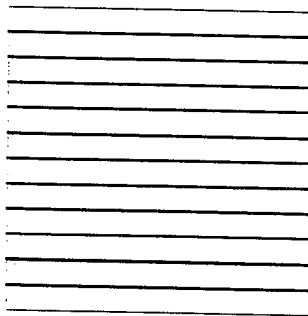
Layer 3

Horizontal



Layer 2

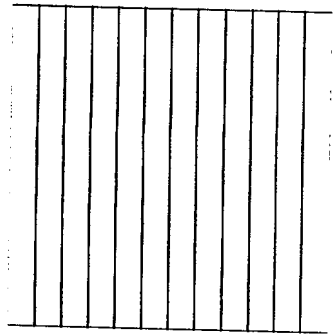
Vertical



Layer 1

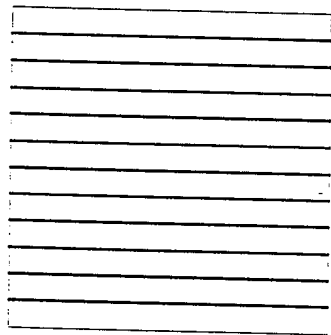
Horizontal

**Figure 6a**



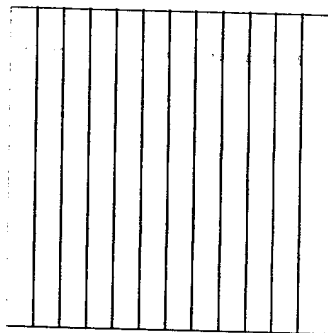
Layer 3

Vertical



Layer 2

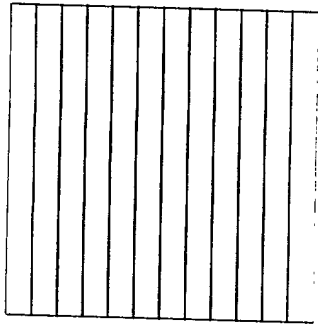
Horizontal



Layer 1

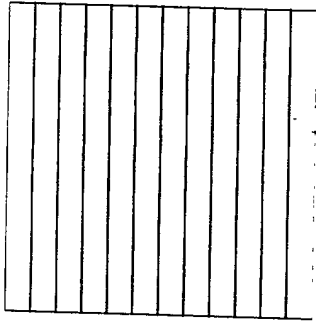
Vertical

**Figure 6b**



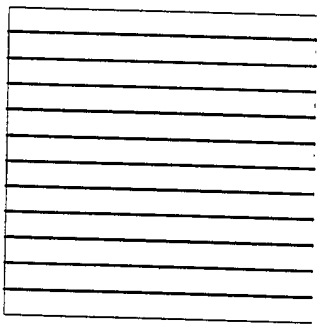
Layer 3

Vertical



Layer 2

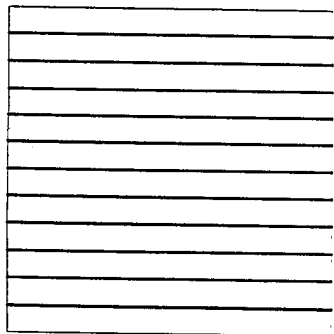
Vertical



Layer 1

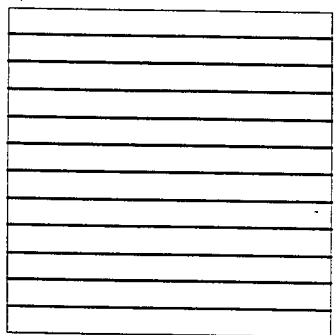
Horizontal

**Figure 6c**



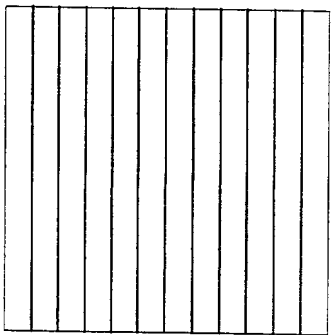
Layer 3

Horizontal



Layer 2

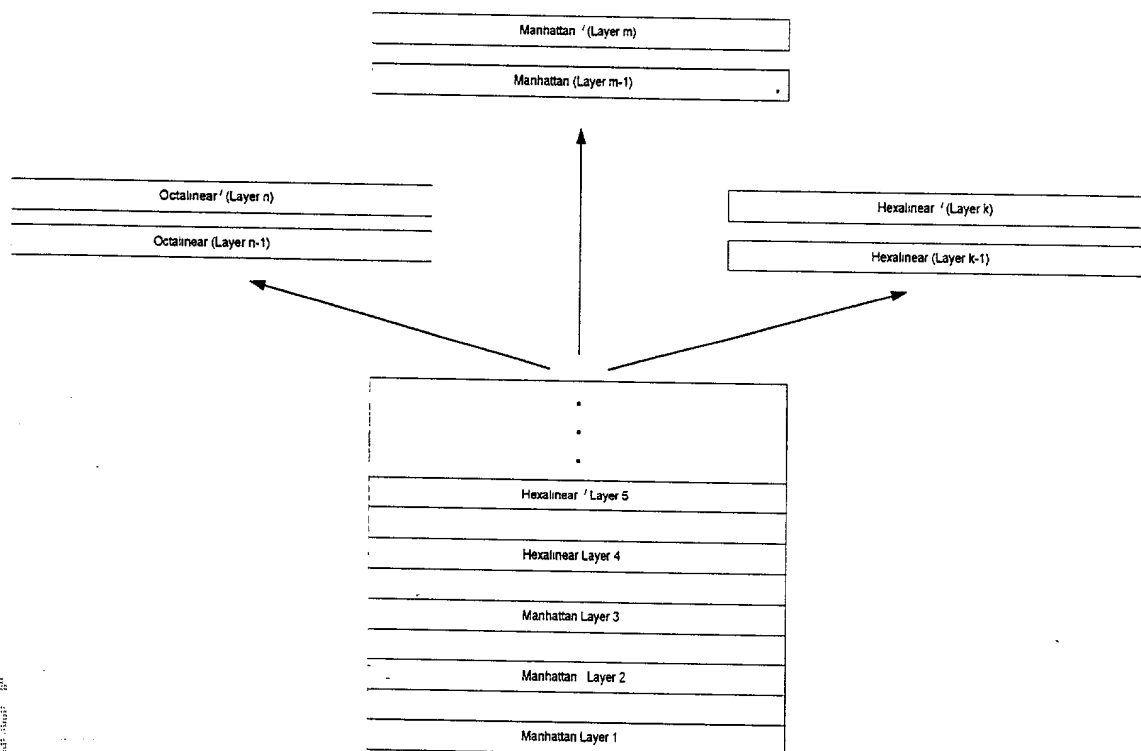
Horizontal



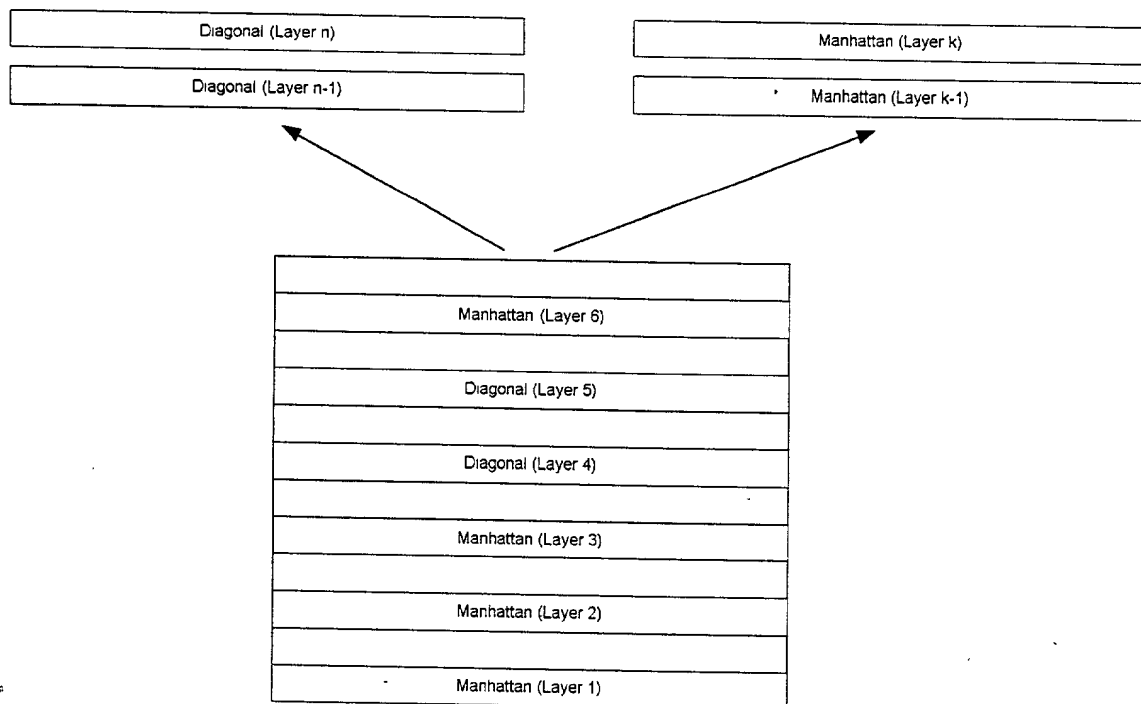
Layer 1

Vertical

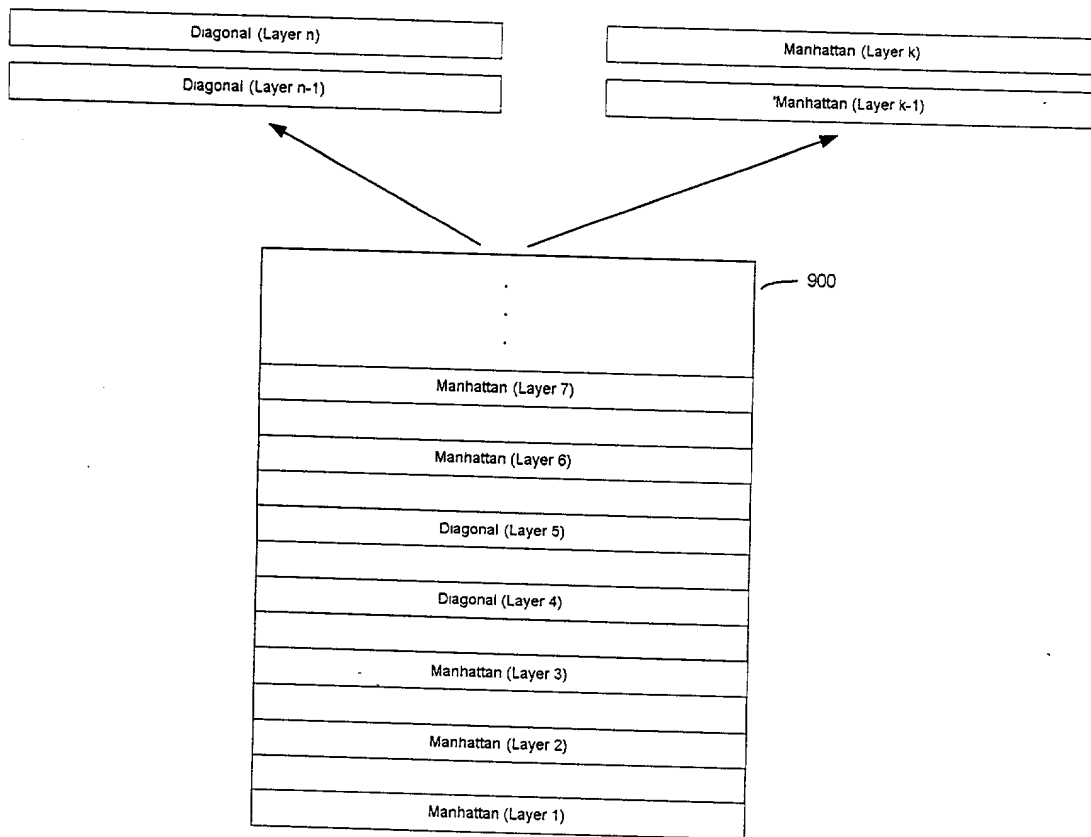
**Figure 6d**



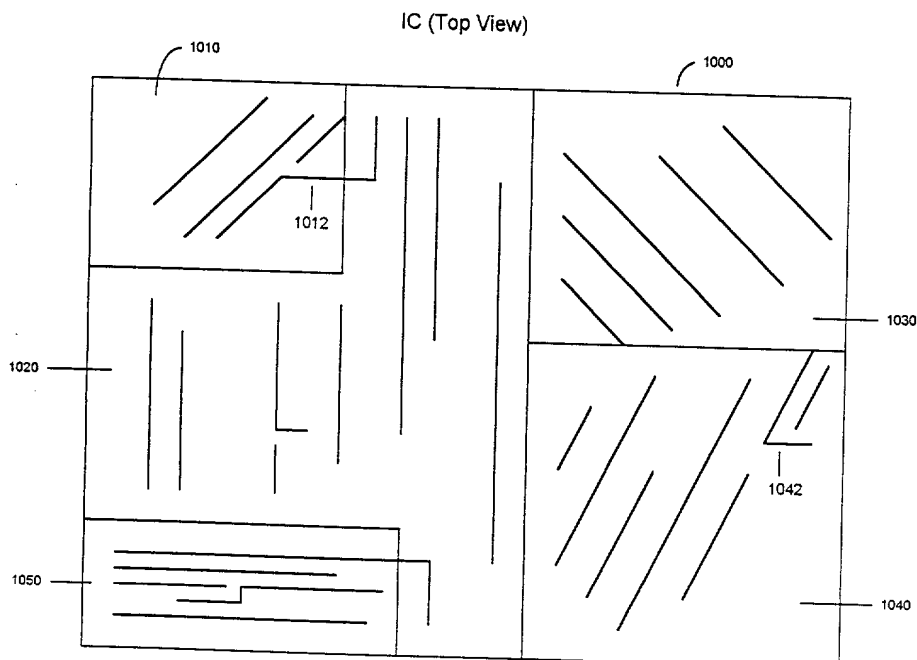
**Figure 7**



**Figure 8**

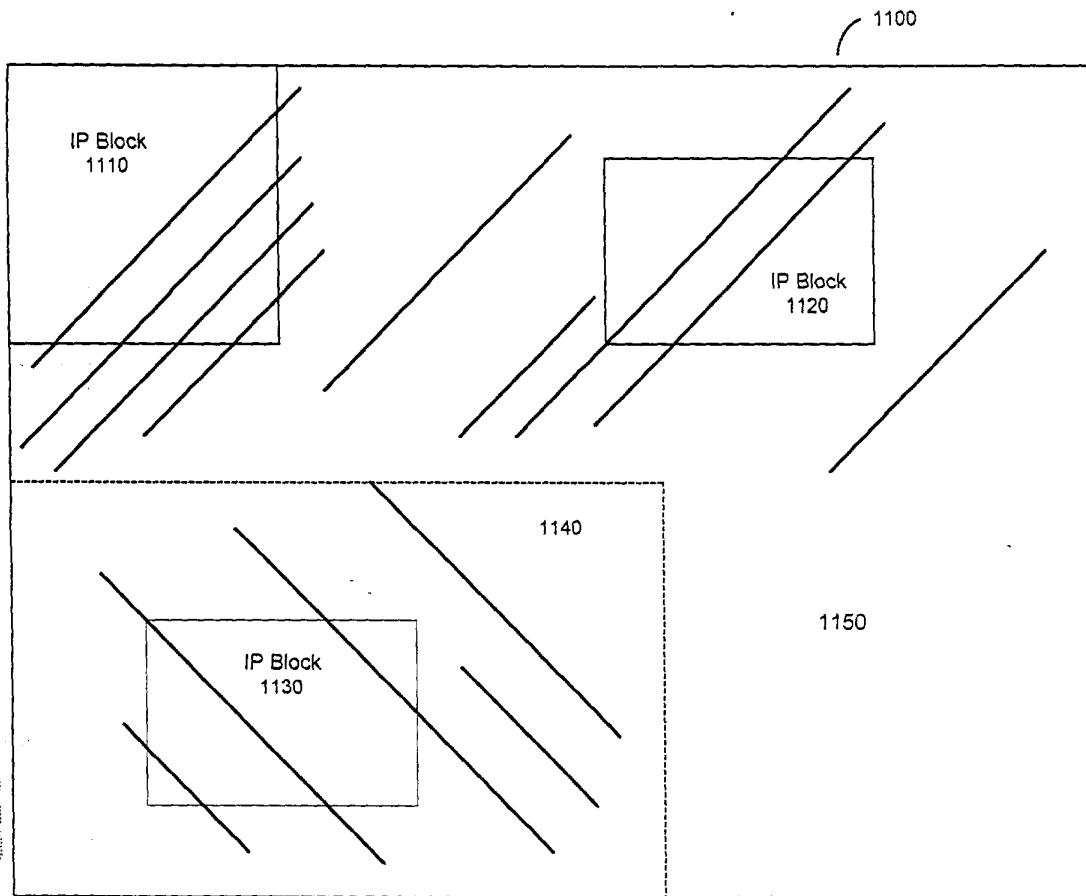


**Figure 9**



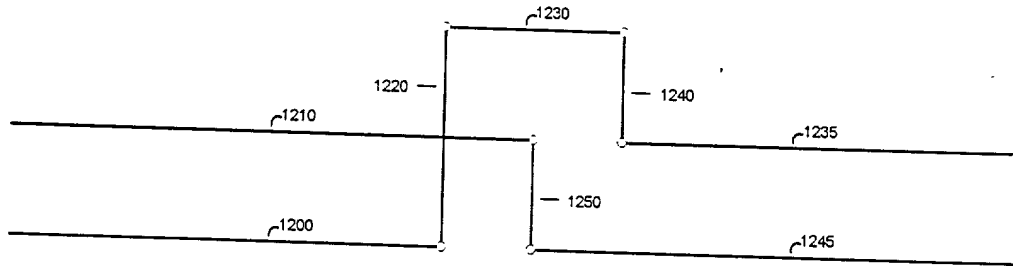
**Figure 10**

IC (Top View)



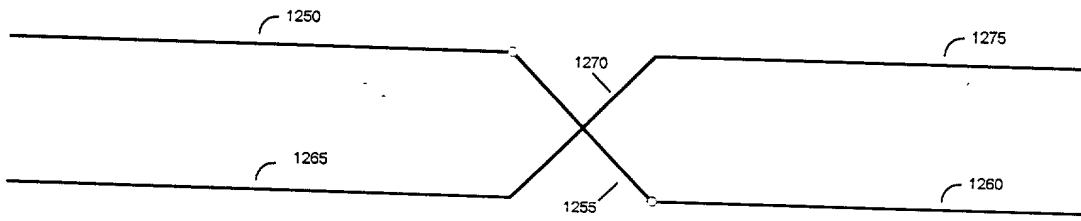
**Figure 11**



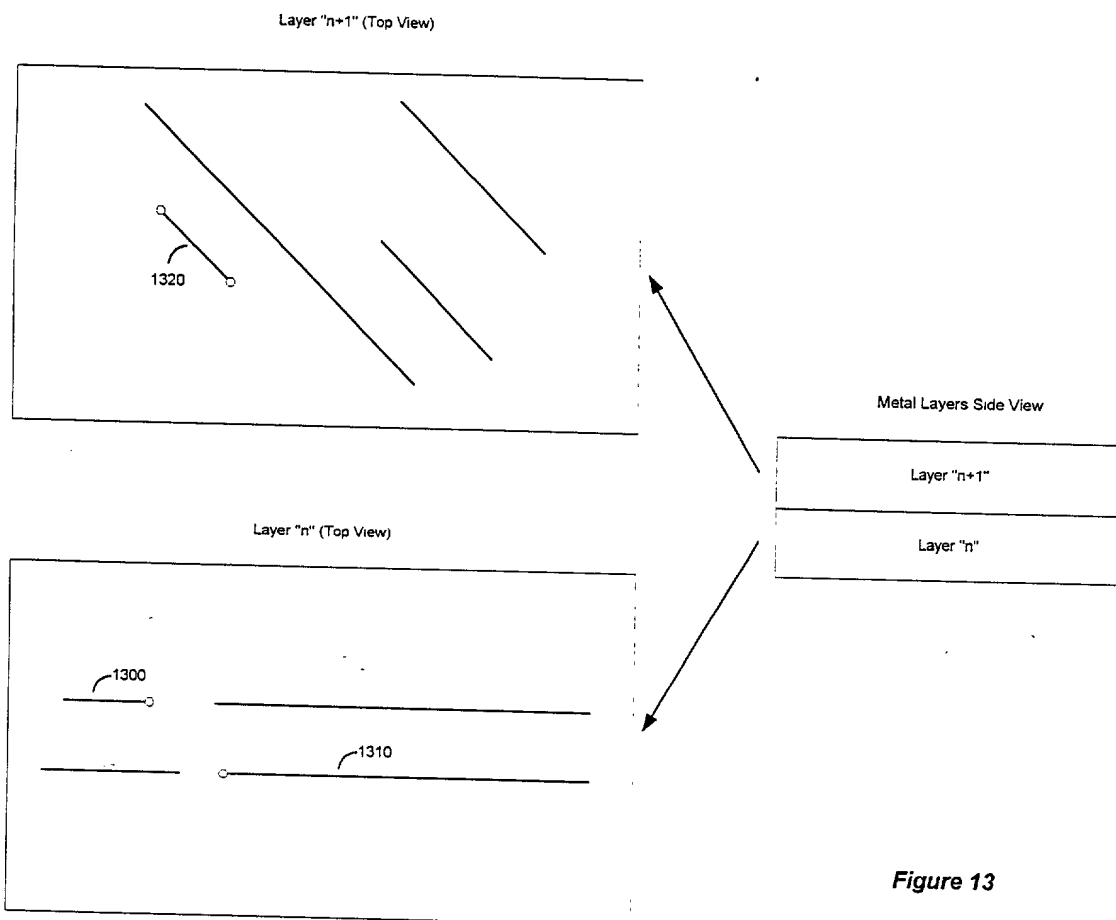


**Figure 12a**

**Prior Art**



**Figure 12b**



**Figure 13**

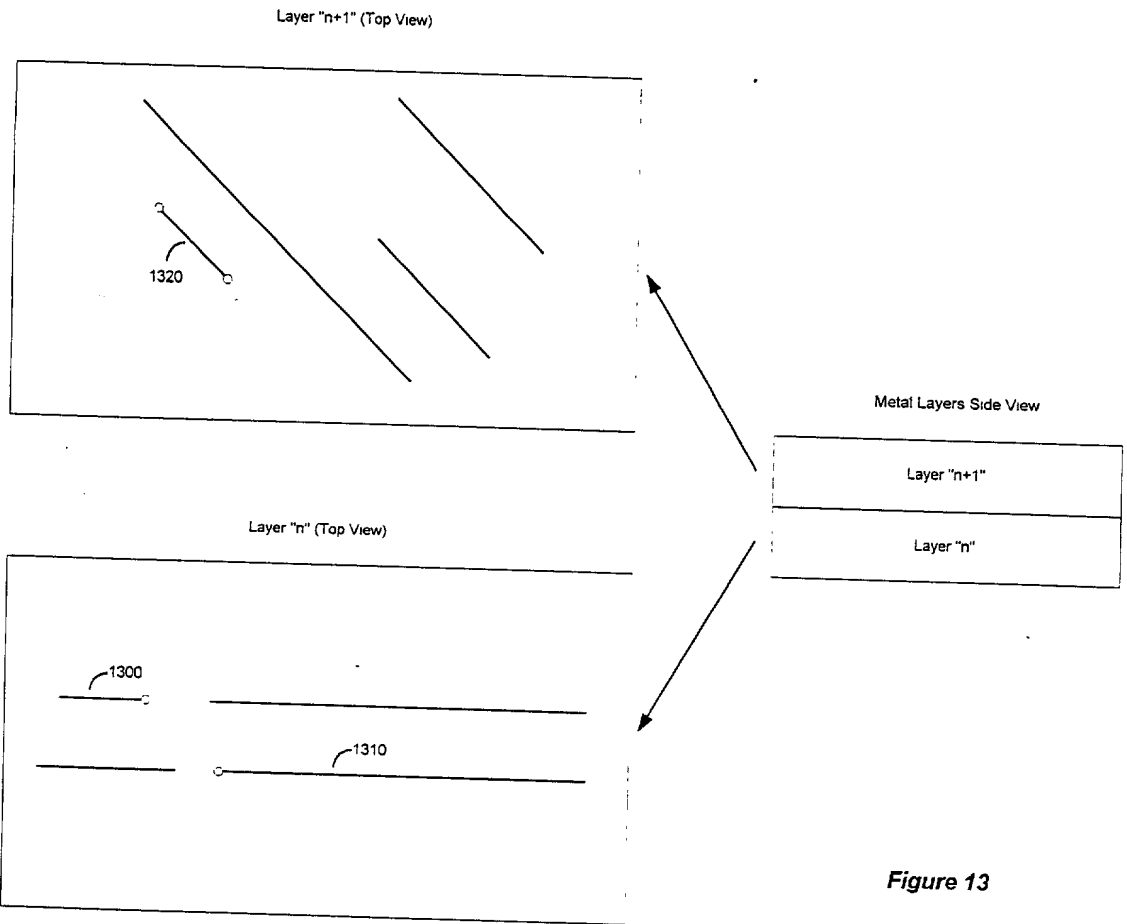


Figure 13

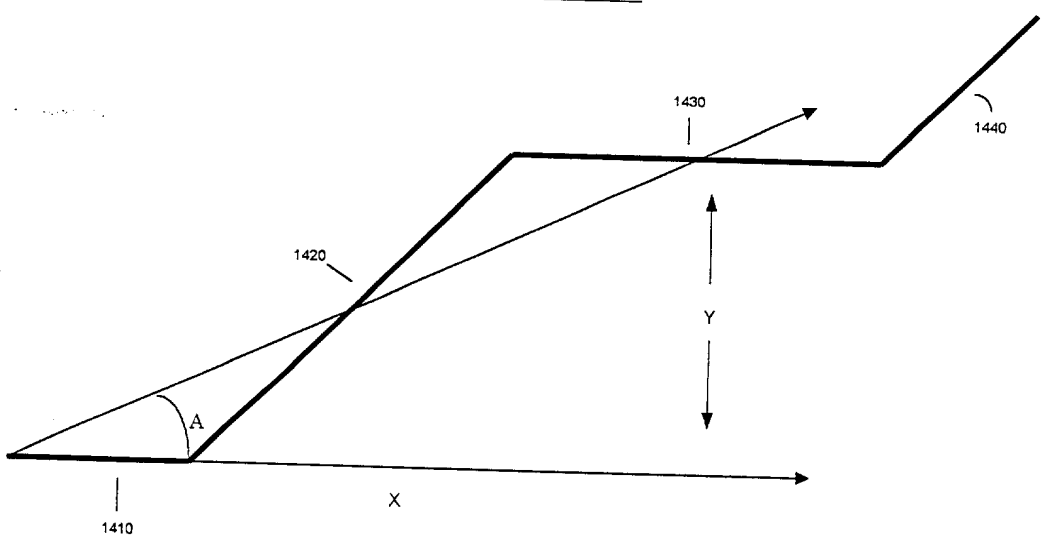
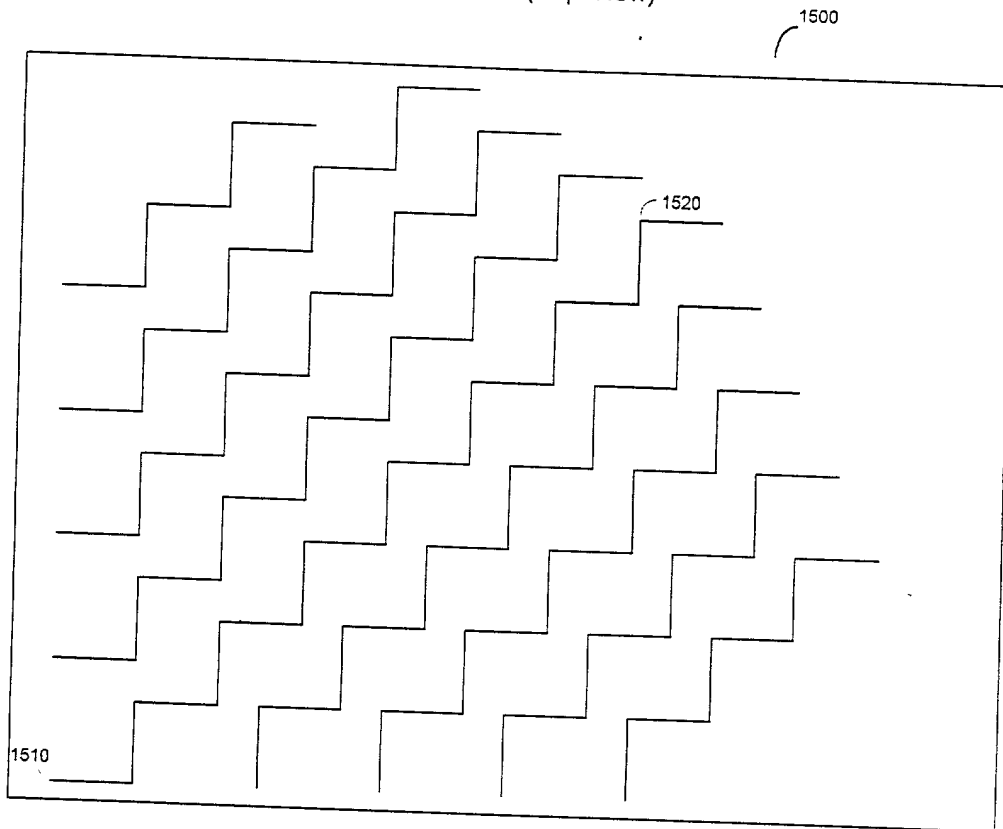


Figure 14

IC (Top View)



**Figure 15**

